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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L STREET NW
WASHINGTON, DC 20037-1526

EXAMINER	
GUHARAY, KARABI	
ART UNIT	**PAPER NUMBER**
2879	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/086,555	RAINA, KANWAL K.	
	Examiner	Art Unit	
	Karabi Guharay	2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Amendment, filed on 4 May 2004, has been considered and entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 24-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cathey et al. (5853492).

Regarding claim 24, Cathey et al. disclose a field emission display device (Fig 1) comprising at least one current emitter (102a) formed of silicon (lines 63-64 of column 2), a substrate (110) having a phosphor coating in at least one region positioned to receive electrons from the current emitters (Column 1, lines 9-20), the treated current emitter surface (treated with wet chemical process) having an atomic concentration of oxygen being smaller than the atomic concentration of oxygen of the current emitter subjected to atmospheric conditions (native oxide present under atmospheric conditions being removed by treatment, thus having less atomic concentration after treatment, lines 34-37 of column 2).

Examiner notes that applicant is claiming the product of field emission display including a method of making the current emitter surface. Consequently, claim 24 is considered as "product by process" claim. In spite of the fact that a product by process claim may recite process limitations, it is the product and not

the recited process that is covered by the claim determines the patentability. Further, patentability of a claim to a product does not rest merely on the difference in the method by which the product is made. See MPEP 2113.

Furthermore, Cathey et al. discloses an alternative method in which a current emitter (silicon emitter, line 64 of column 2) is treated by wet chemical process resulting in reduction of native oxides (silicon dioxide).

But, Cathey is silent about current emitter being doped. However, it is well known that silicon materials when used as emitters are doped with N-type materials in order to accord low work function and to decrease electrical resistivity.

Thus it would have been obvious to one having ordinary skill in the art at the time the invention was made to use doped silicon as the electron emitter material in the device of Cathey, since this will lower the work-function of the emitter.

Regarding claim 25, Cathey et al. disclose that the native oxides (which is silicon dioxide, in case of silicon emitter) are removed from the silicon emitter (line 64 of column 2) surface thus resulting a reduced concentration of oxygen and silicon (lines 34-37 of column 2).

Regarding claim 26, Cathey et al. disclose a field emission display device (Fig 1) comprising at least one current emitter (102a) formed of silicon (lines 63-64 of column 2), a substrate (110) having a phosphor coating in at least one region positioned to receive electrons from the current emitters (lines 9-20 of Column 1), the current emitter comprising a treated emission surface having

native oxides removed from the surface thus reducing atomic concentration of oxygen (lines 24-37 of column 2).

Furthermore, examiner notes that applicant is claiming the product of field emission display including a method of making the current emitter surface. Consequently, claim 26 is considered as "product by process" claim. In spite of the fact that a product by process claim may recite process limitations, it is the product and not the recited process that is covered by the claim determines the patentability. Further, patentability of a claim to a product does not rest merely on the difference in the method by which the product is made. See MPEP 2113.

Furthermore, Cathey et al. discloses an alternative method in which a current emitter is treated by wet chemical process resulting in reduction of native oxides.

But, Cathey is silent about current emitter being doped. However, it is well known that silicon materials when used as emitters are doped with N-type materials in order to accord low work function and to decrease electrical resistivity.

Thus it would have been obvious to one having ordinary skill in the art at the time the invention was made to use doped silicon as the electron emitter material in the device of Cathey, since this will lower the work-function of the emitter.

Regarding claim 27, Cathey et al. disclose a field emission display device (Fig 1) comprising at least one current emitter (102a) formed of doped silicon (lines 63-64 of column 2), a substrate (110) having a phosphor coating in at least

one region positioned to receive electrons from the current emitters (Column 1, lines 9-20), the current emitter comprising a treated emission surface having native oxides removed from the surface, thus reducing the atomic concentration of oxygen compared to oxygen concentration under atmospheric condition(lines 24-37 of column 2).

Furthermore, examiner notes that applicant is claiming the product of field emission display including a method of making the current emitter surface. Consequently, claim 27 is considered as "product by process" claim. In spite of the fact that a product by process claim may recite process limitations, it is the product and not the recited process that is covered by the claim determines the patentability. Further, patentability of a claim to a product does not rest merely on the difference in the method by which the product is made. See MPEP 2113.

Furthermore, Cathey et al. discloses an alternative method in which a current emitter is treated by wet chemical process resulting in reduction of native oxides.

But, Cathey is silent about current emitter being doped. However, it is well known that silicon materials when used as emitters are doped with N-type materials in order to accord low work function and to decrease electrical resistivity.

Thus it would have been obvious to one having ordinary skill in the art at the time the invention was made to use doped silicon as the electron emitter material in the device of Cathey, since this will lower the work-function of the emitter.

Regarding claim 28, Cathey et al. disclose a field emission display device (Fig 1) comprising at least one current emitter (102a) formed of silicon (lines 63-64 of column 2), a substrate (110) having a phosphor coating in at least one region positioned to receive electrons from the current emitters (Column 1, lines 9-20), the current emitter comprising a treated emission surface (wet treated) having native oxides removed from the surface thus resulting a smaller atomic concentration of oxygen than the oxygen concentration of the electron emission surface subjected to atmospheric conditions, which produce native oxides (lines 24-37 of column 2).

But, Cathey is silent about current emitter being doped. However, it is well known that silicon materials when used as emitters are doped with N-type materials in order to accord low work function and to decrease electrical resistivity.

Thus it would have been obvious to one having ordinary skill in the art at the time the invention was made to use doped silicon as the electron emitter material in the device of Cathey, since this will lower the work-function of the emitter.

Regarding claim 29, Cathey et al. disclose a field emission display device (Fig 1) comprising at least one current emitter (102a) formed of doped silicon (lines 63-64 of column 2), a substrate (110) having a phosphor coating in at least one region positioned to receive electrons from the current emitters (lines 9-20 of Column 1), the current emitter comprising a treated emission surface (wet

chemical treatment) which removes native oxides on the silicon surface, thus reduces concentration of silicon (since native oxides are silicon dioxide) than the silicon concentration of the electron emission surface subjected to atmospheric conditions, which produce native oxides (lines 24-37 of column 2).

But, Cathey is silent about current emitter being doped. However, it is well known that silicon materials when used as emitters are doped with N-type materials in order to accord low work function and to decrease electrical resistivity.

Thus it would have been obvious to one having ordinary skill in the art at the time the invention was made to use doped silicon as the electron emitter material in the device of Cathey, since this will lower the work-function of the emitter.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 12, and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cathey et al. (US 5853492), and further in view of Jones (US 5371431).

Regarding claim 12, Cathey et al. disclose a field emission display device (Fig 1) comprising at least one current emitter (102a) formed of doped silicon

(lines 63-64 of column 2) a substrate (110) having a phosphor coating in at least one region positioned to receive electrons from the current emitters (Column 1, lines 9-20), the current emitter comprising a treated emission surface having an atomic concentration of oxygen smaller than atomic concentration under atmospheric conditions (lines 24-37 of column 2).

Furthermore, examiner notes that applicant is claiming the product of field emission display including a method of making the current emitter surface. Consequently, claim 12 is considered a "product by process" claim. In spite of the fact that a product by process claim may recite process limitations, it is the product and not the recited process that is covered by the claim determines the patentability. Further, patentability of a claim to a product does not rest merely on the difference in the method by which the product is made. See MPEP 2113.

But, Cathey is silent about current emitter being doped. However, it is well known that silicon materials when used as emitters are doped with N-type materials in order to accord low work function and to decrease electrical resistivity.

Thus it would have been obvious to one having ordinary skill in the art at the time the invention was made to use doped silicon as the electron emitter material in the device of Cathey, since this will lower the work-function of the emitter.

Cathey et al. further disclose that the electron emitter comprises sides, but fail to disclose that at least a portion of the sides being surrounded by an insulating layer (106) to prevent current from radiating out of the sides (Fig 1).

However, Jones discloses a field emission device (Fig 8, or Fig 11C) including electron emitter (metal column 12 with tip 15) having at least a portion of the sides of the emitter surrounded by an insulating layer (19, lines 14-18 of column 12), insulating layer touching the sides of the emitter column 12 (see Fig 11C), thus preventing current from radiating out of the sides. This type of configuration of emitters and the insulating layer reduce the parasitic capacitance of the emitter and prevent charge transfer between the emitters (lines 17-20 of column 3).

Thus it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide insulating layer surrounding at least a portion of the sides of the electron emitter, as disclosed by Jones, in the device of Cathey et al., since this will reduce the parasitic capacitance of the emitter and also prevent charge transfer between emitters.

Regarding claim 18, Jones discloses that the current emitter comprises a tip (15) and the sides (sides of column 12) do not include any portion of the tip 15 (see Fig 8, Fig 10E). The same reason for combining art as in claim 12 applies.

Regarding claim 19, Jones discloses that the insulating layer 19 includes silicon dioxide (Column 6, lines 34-35). The same reason for combining art as in claim 12 applies.

Claims 13-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cathey '492 and Jones '431 as applied to claim 12 above, and further in view of Yamazaki (US 5840118).

Regarding claim 13, Jones discloses that the substrate (11) is a glass substrate (lines 12-14 of column 14) but fails to disclose a barrier film on the substrate.

However, Yamazaki teaches a glass substrate covered with a barrier film in order to prevent scattering of impurities from the glass substrate (lines 4-8 of column 5).

Thus it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate a barrier film covering the glass substrate, as disclosed by Yamazaki, so that scattering of impurities from the glass substrate can be prevented.

Regarding claim 14, Yamazaki discloses that the barrier film comprises silicon dioxide (line 6 of column 5).

Regarding claim 15, Jones discloses that the current emitter has a base (12) on the barrier layer of the combined structure and a projecting top 15 connected with the base 12 (see Fig 11c).

Regarding claim 16, Jones discloses a conductive layer (17) deposited on the barrier layer of the combined structure (see Fig 8).

Regarding claim 17, Jones discloses that conductive layer (17) is a metal layer (lines 40-43 of column 8), but silent about particular metal. However, it is well known that aluminum is a suitable metal widely used for conductive layer.

Further It is noted that applicant's specific metal, aluminum does not solve any of the stated problems or yield any unexpected result that is not within the scope of the teachings applied. Therefore it is considered to be a matter of

choice, which a person of ordinary skill in the art would have found obvious to select aluminum as the material for the conductive layer (17).

Claims 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cathey '492 and Jones '431 as applied to claim 12 above, and further in view of Cathey (US 6020683).

Regarding claim 20-21, Cathey and Jones fail to disclose that silicon grid resides on the insulating layer (as claimed in claim 20) and further a metal layer resides on silicon grid layer (as claimed in claim 21).

However, Cathey in '683 discloses a field emission display device (Fig 2) having a silicon grid (42, line 10 of column 6) then a metal layer (60) on top of silicon grid on top of metal layer 60 in order to control operation of grid (lines 59-63 of column 4).

Thus it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a silicon grid and a metal layer on top of the silicon grid as disclosed by Cathey in patent '683 in the combined structure of Cathey and Jones in order to control operation of grid or other circuit components.

Regarding claim 22, Jones discloses a passivation layer (54) on top of the grid (47 see Fig 8).

Regarding claim 23, Jones discloses that the passivation layer (54) comprises nitride.

Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sandhu et al. (US 6086442), further in view of Jones (US 5371431).

Regarding claim 30, Sandhu et al. disclose a field emission display device (Fig 3) comprising at least one current emitter (48) formed of doped silicon (Column 2, lines 20-23), a substrate (60) having a phosphor coating (62) in at least one region positioned to receive electrons from the current emitters (Column 4, lines 46-57), the current emitter comprising a treated (selectively depositing) current emission surface (56) from treatment (selectively depositing) of the current emission surface followed by nitridation process to form metal nitride by exposing the surface to nitrogen plasma (lines 52 of column 2-23 of column 3), thus inherently resulting greater nitrogen concentration than the silicon emitter exposed to atmosphere.

Sandhu et al. further disclose that the electron emitter comprises sides, but fail to disclose that at least a portion of the sides being surrounded by an insulating layer to prevent current from radiating out of the sides (Fig 3).

However, Jones discloses a field emission device (Fig 8, or Fig 11C) including electron emitter (metal column 12 with tip 15) having at least a portion of the sides of the emitter surrounded by an insulating layer (19, lines 14-18 of column 12), insulating layer touching the sides of the emitter column 12 (see Fig 11C), thus preventing current from radiating out of the sides. This type of configuration of emitters and the insulating layer reduce the parasitic capacitance of the emitter and prevent charge transfer between the emitters (lines 17-20 of column 3).

Thus it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide insulating layer surrounding at least a

portion of the sides of the electron emitter, as disclosed by Jones, in the device of Sandhu et al., since this will reduce the parasitic capacitance of the emitter and also prevent charge transfer between emitters.

Response to Arguments

Applicant's argument have been considered but are moot in view of the new ground(s) of rejection.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Karabi Guharay whose telephone number is (571) 272-2452. The examiner can normally be reached on Monday-Friday 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimeshkumar D. Patel can be reached on (571) 272-2457. The fax phone number for the organization is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Karabi Guharay
Karabi Guharay
Patent Examiner
Art Unit 2879